

FIG. 1c (PRIOR ART)

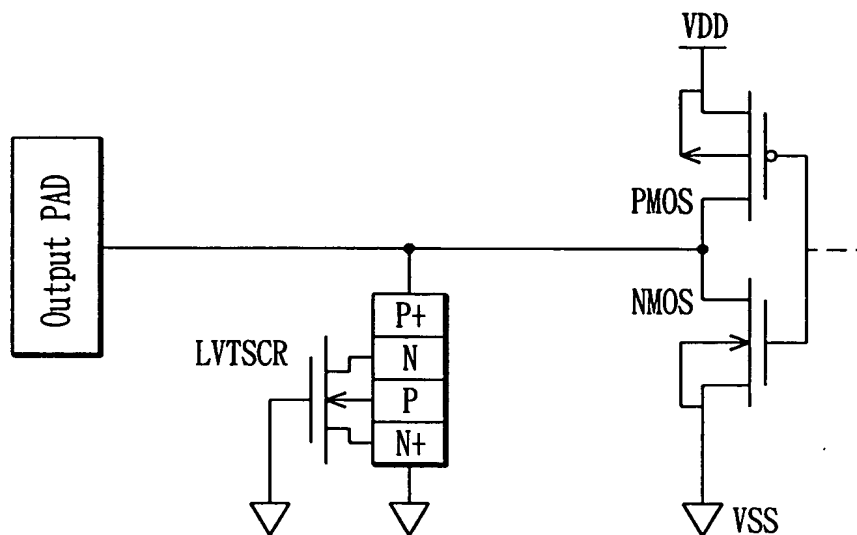


FIG. 2a (PRIOR ART)

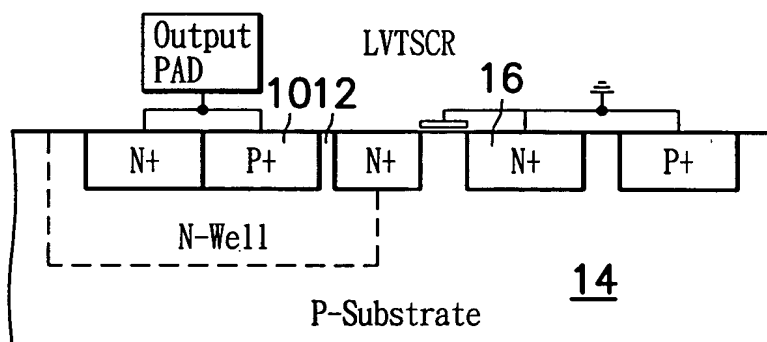


FIG. 2b (PRIOR ART)

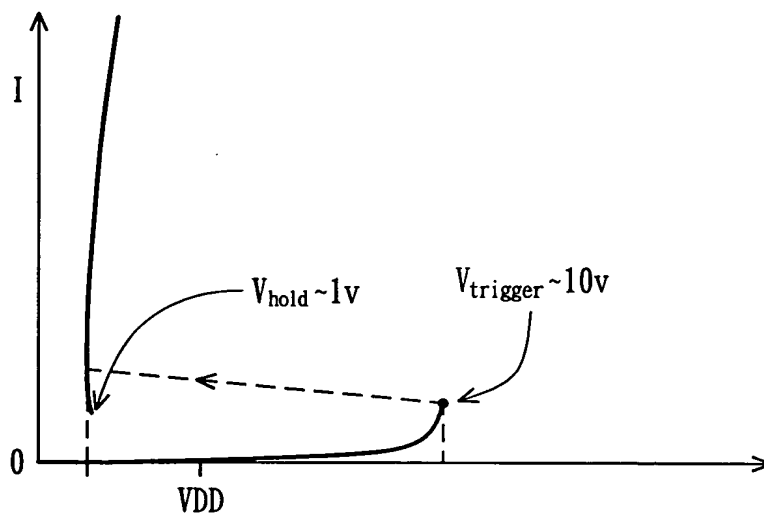
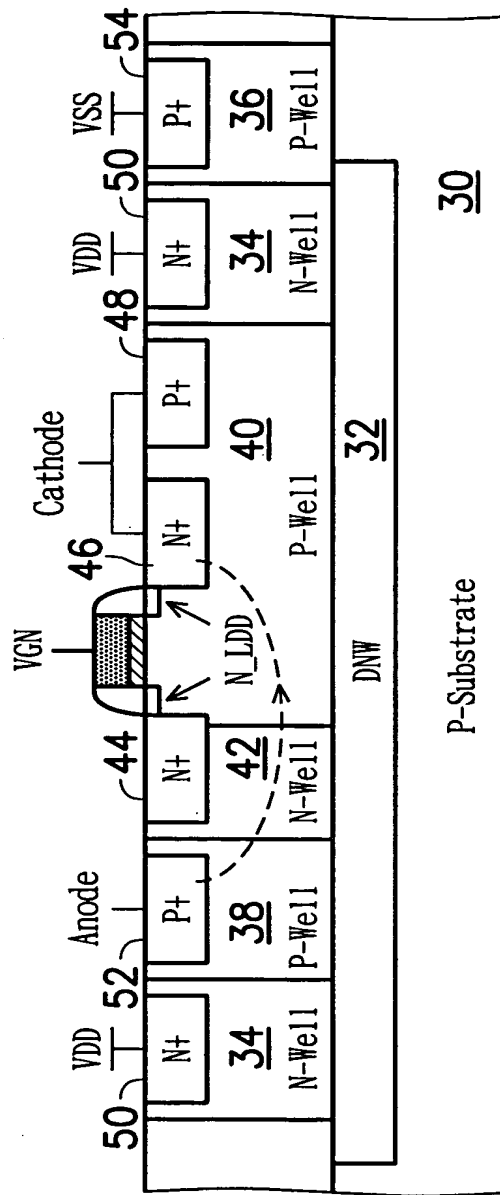


FIG. 2c (PRIOR ART)



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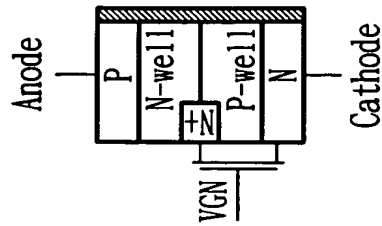
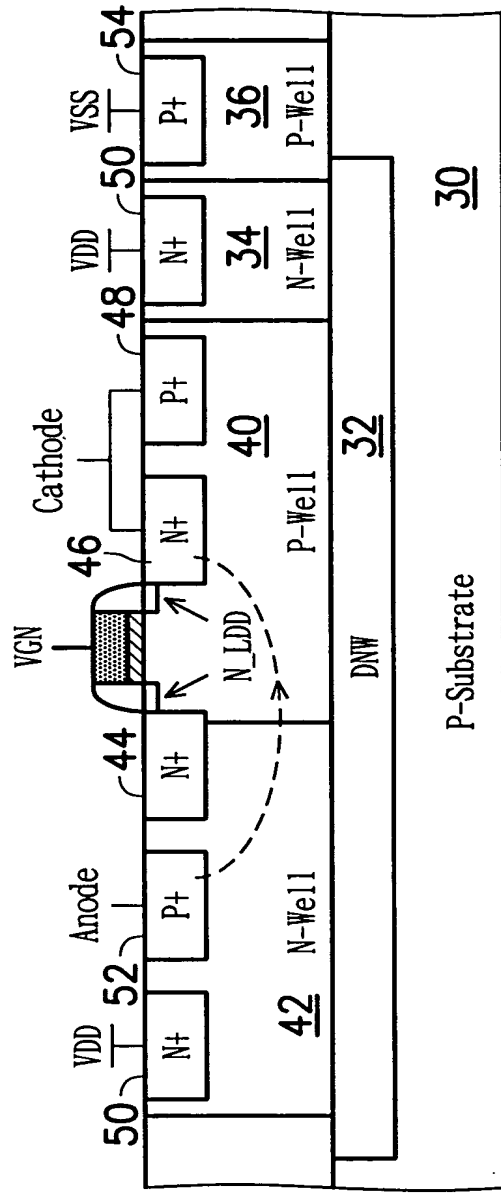


FIG. 3a



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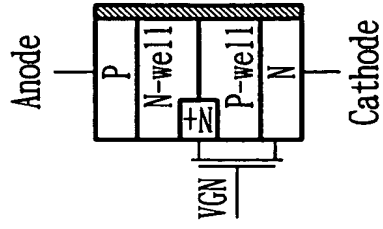
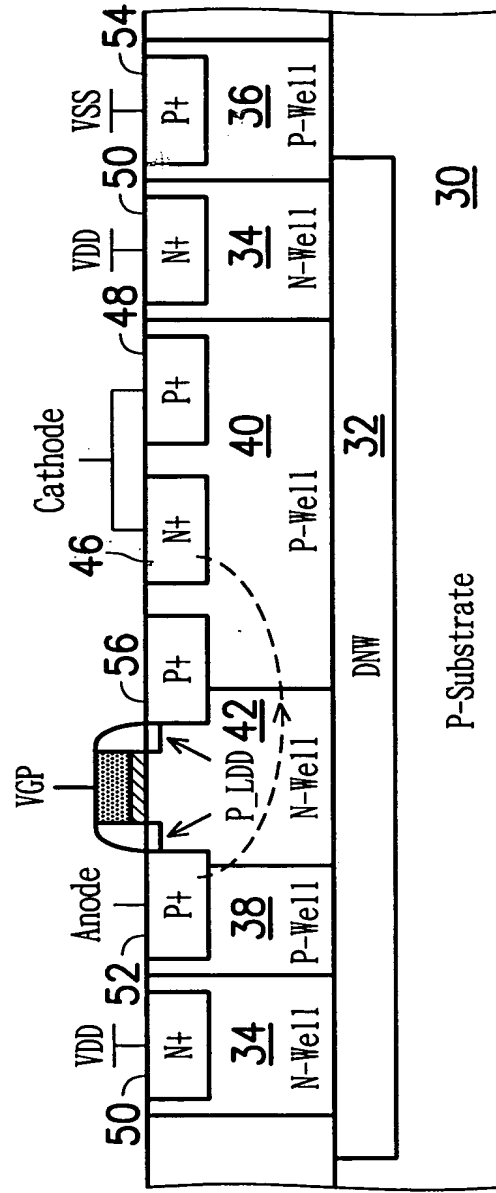


FIG. 3b



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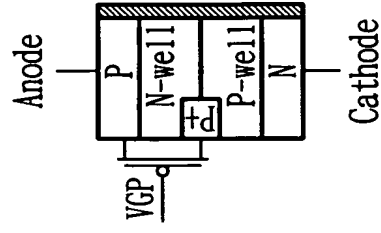


FIG. 4a

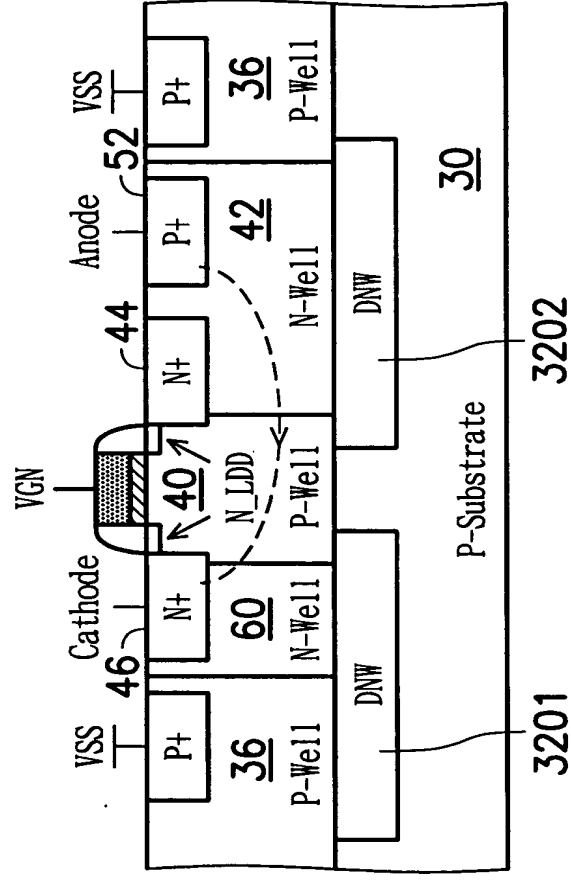


FIG. 5

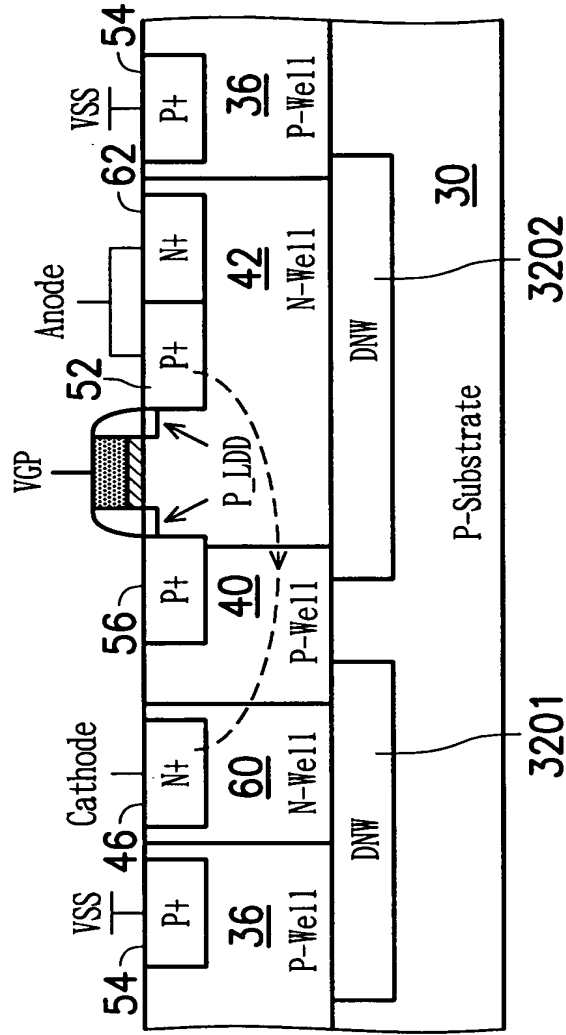


FIG. 6

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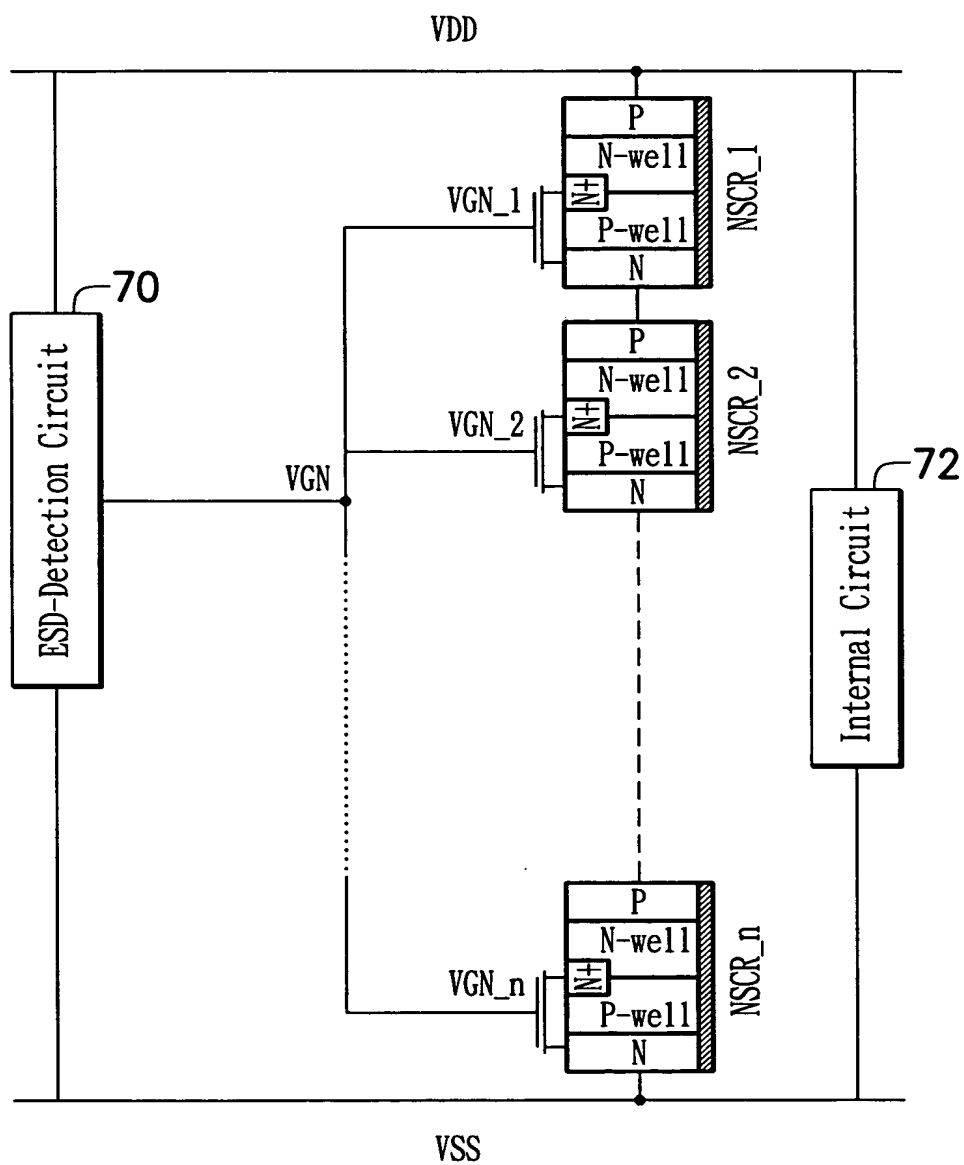


FIG. 7

FIG. 8

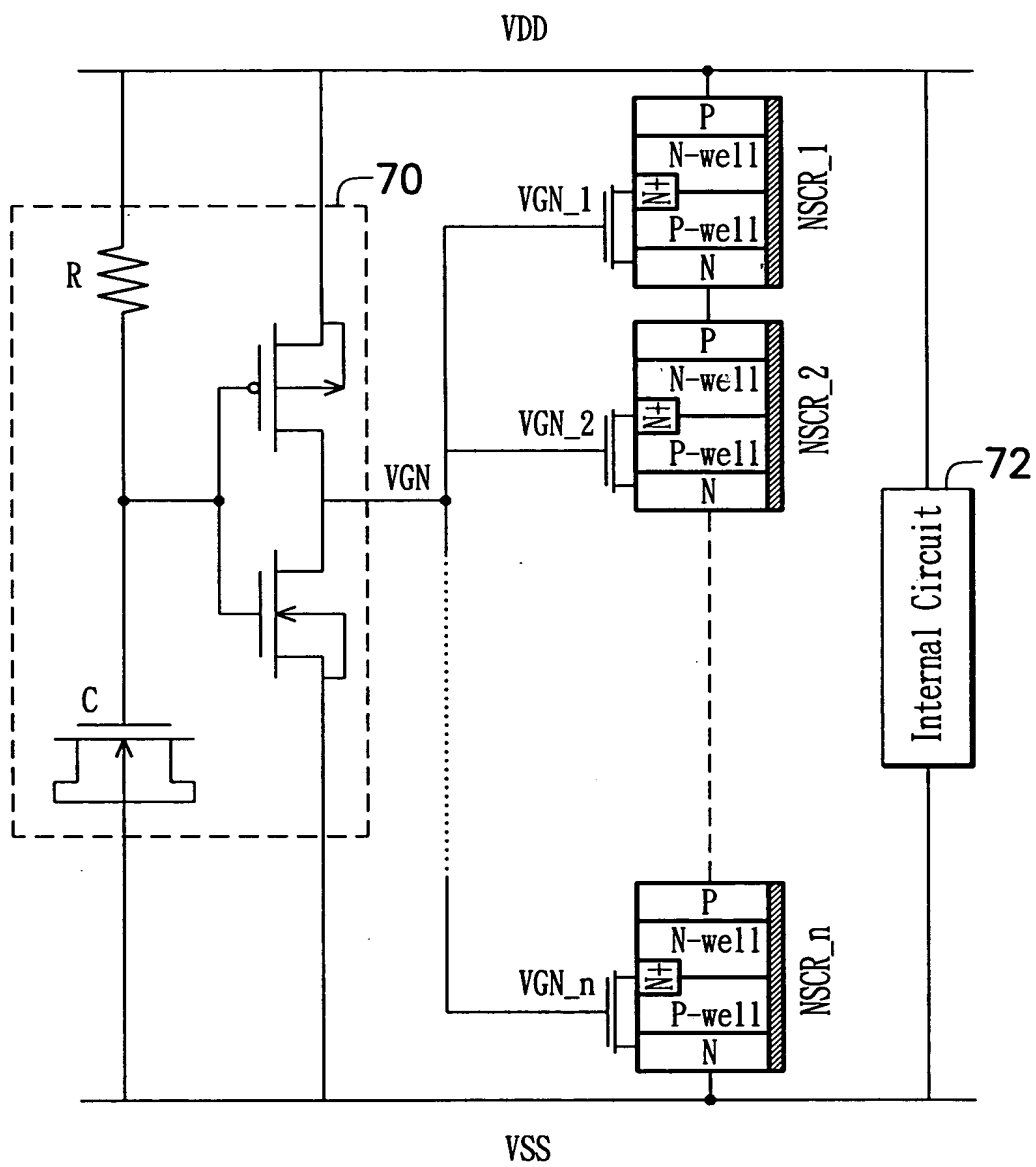


FIG. 8

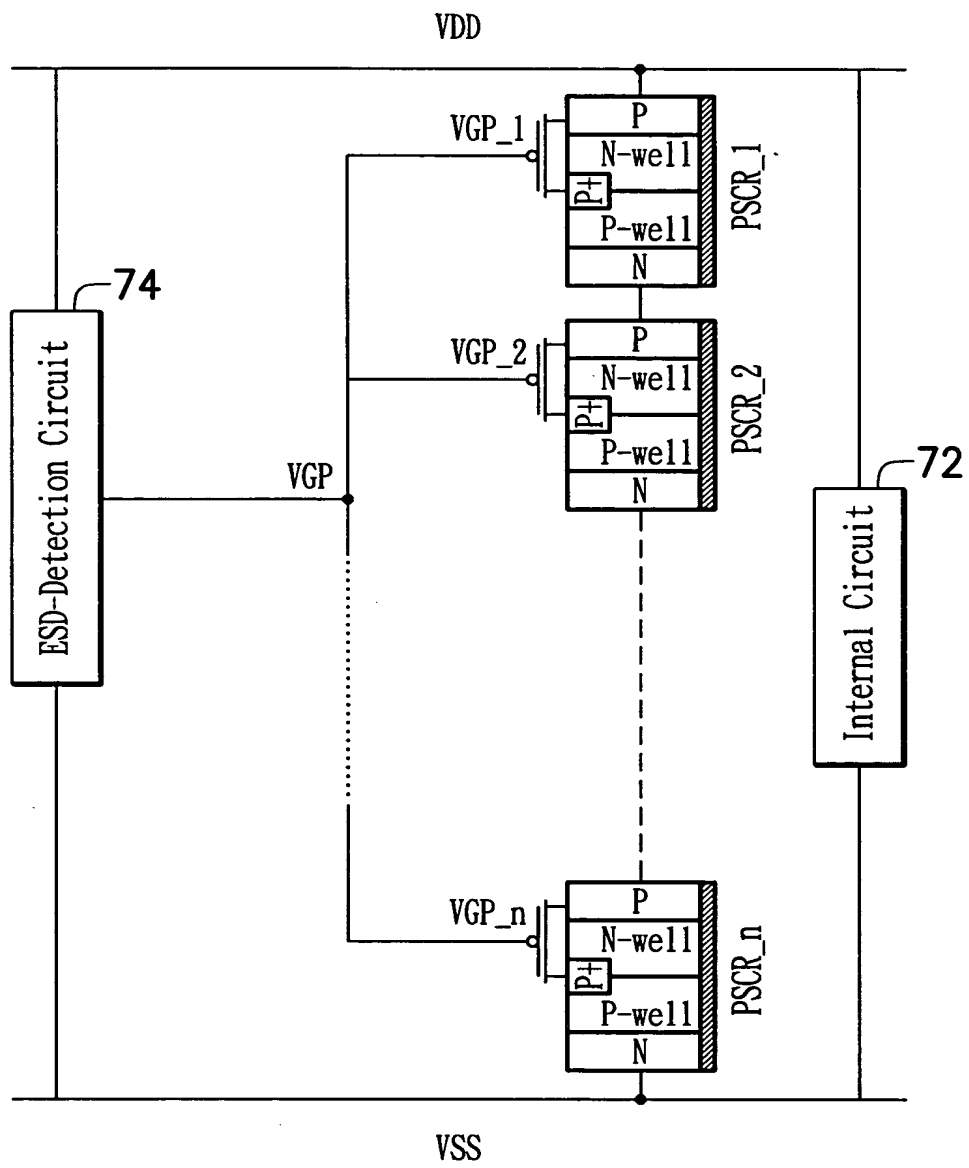


FIG. 9

The diagram shows a circuit 72 with a resistor R and a capacitor C connected to a node VGP. This node VGP is connected to a series of PMOS transistors (PSCR_1, PSCR_2, ..., PSCR_n) which are connected to VDD and VSS. The gates of these PMOS transistors are controlled by VGP_1, VGP_2, ..., VGP_n. The circuit is also connected to an Internal Circuit block.

FIG. 10

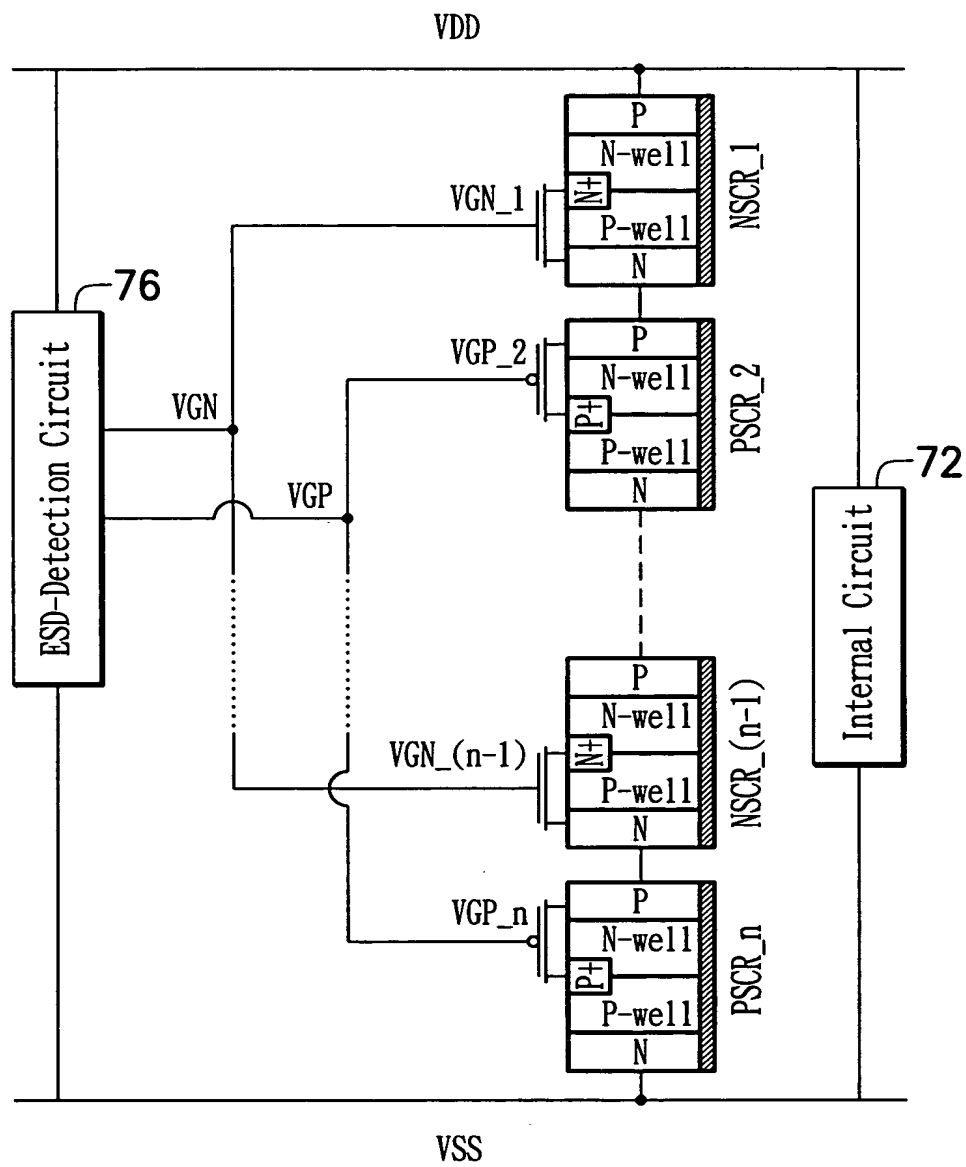


FIG. 11

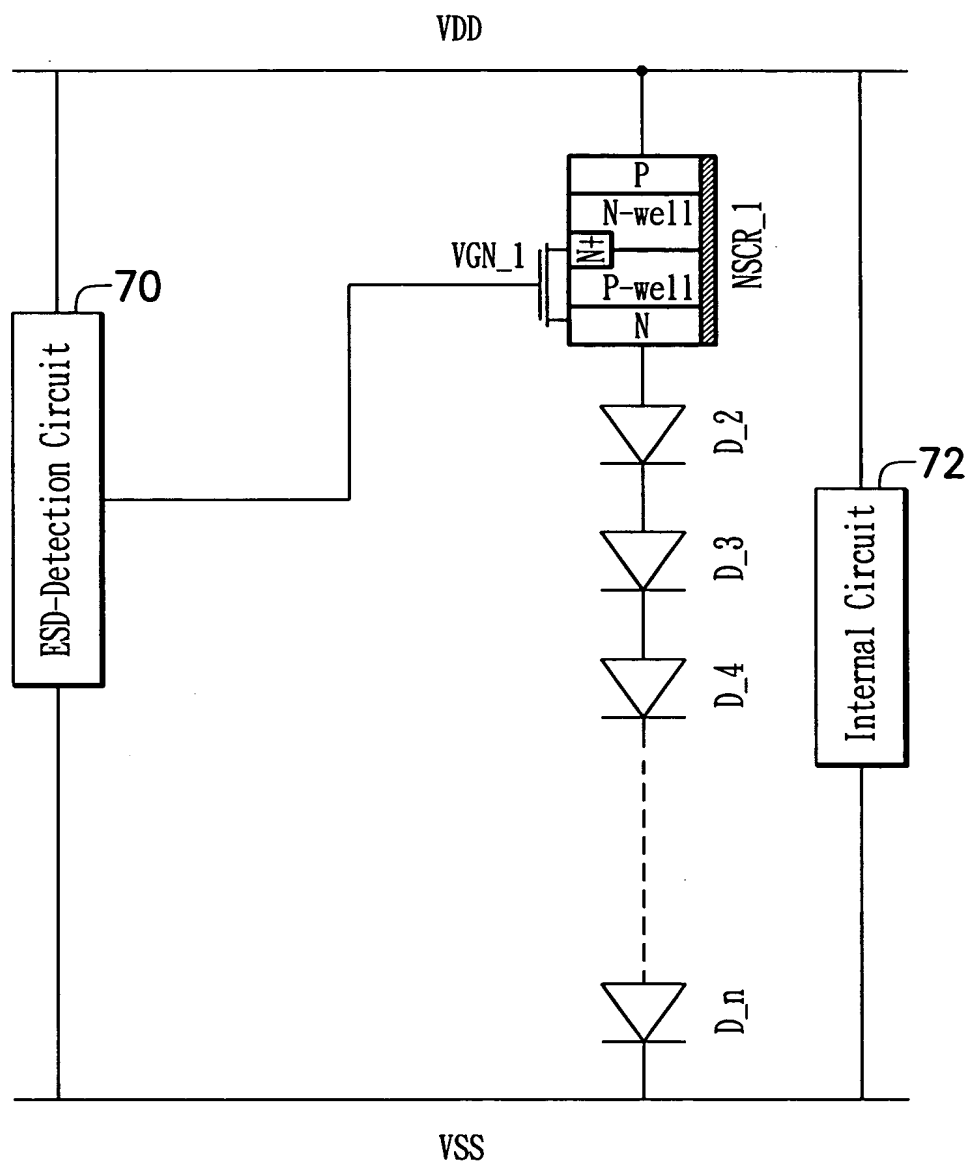


FIG. 12

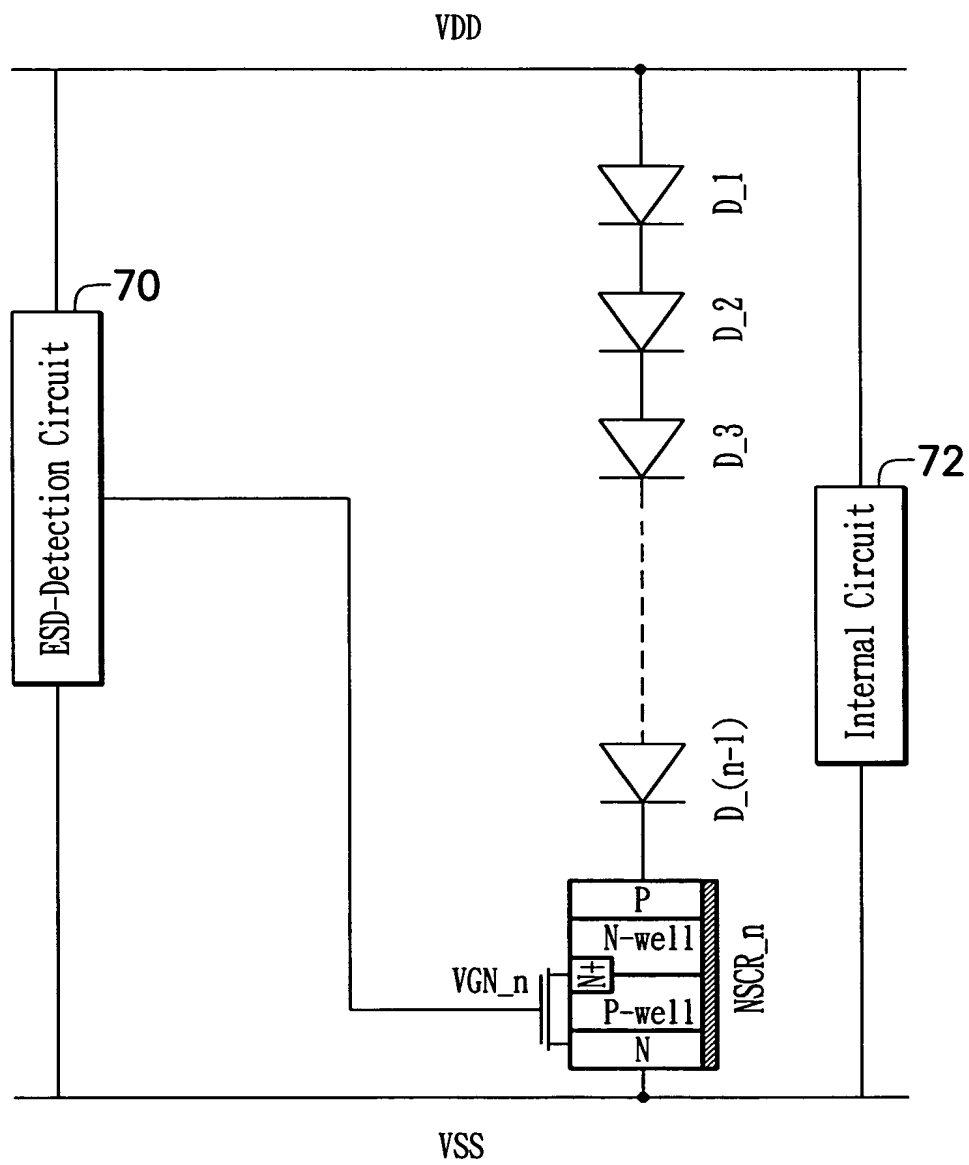


FIG. 13

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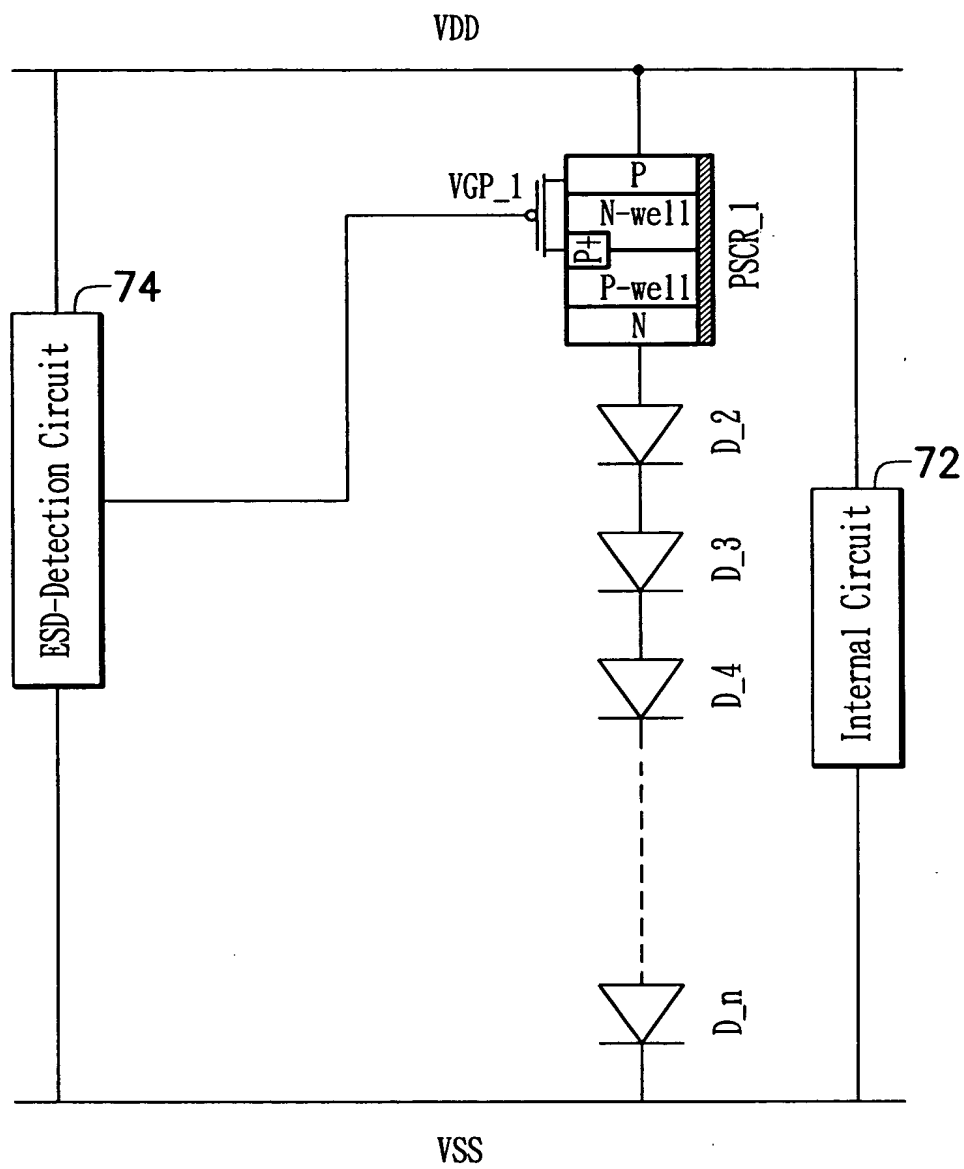


FIG. 14

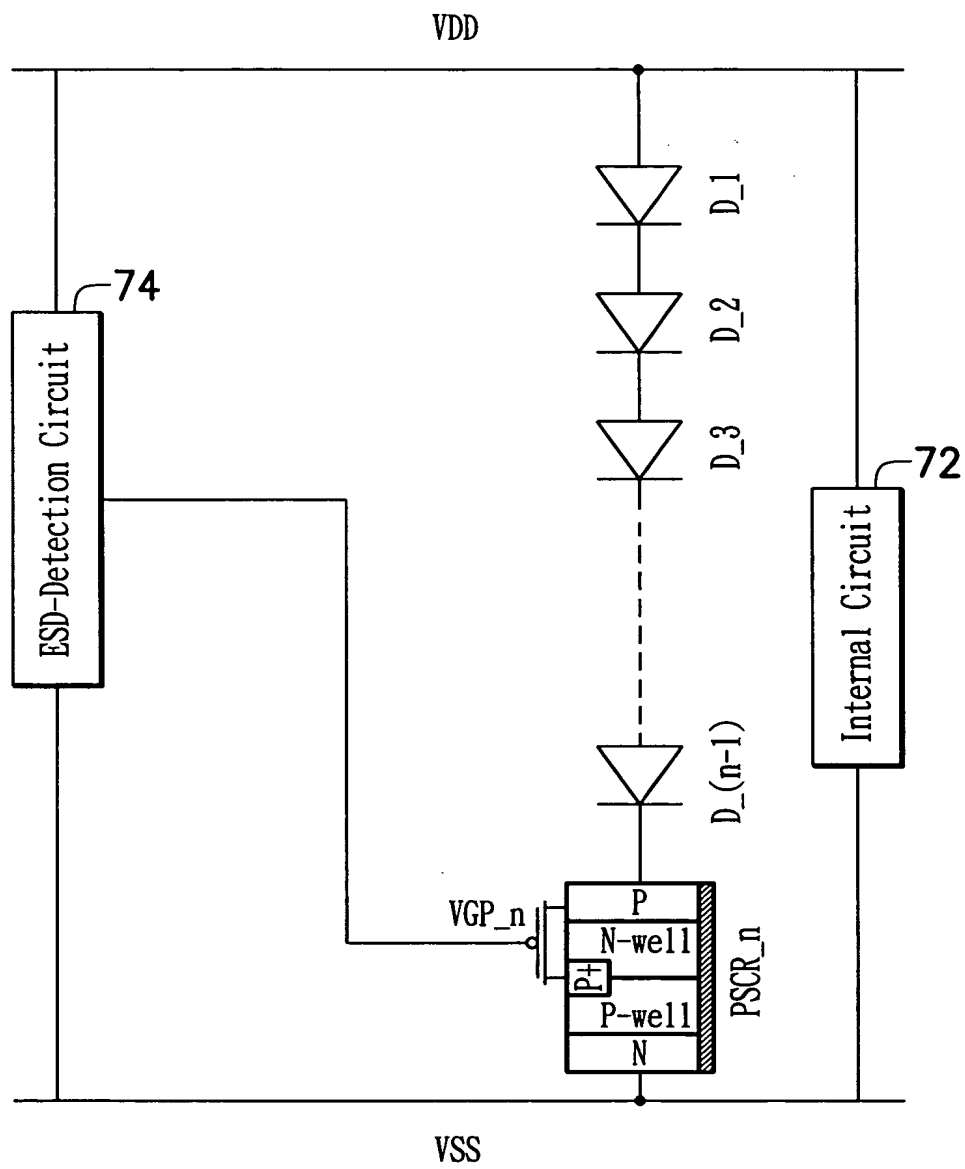


FIG. 15

FIG. 16

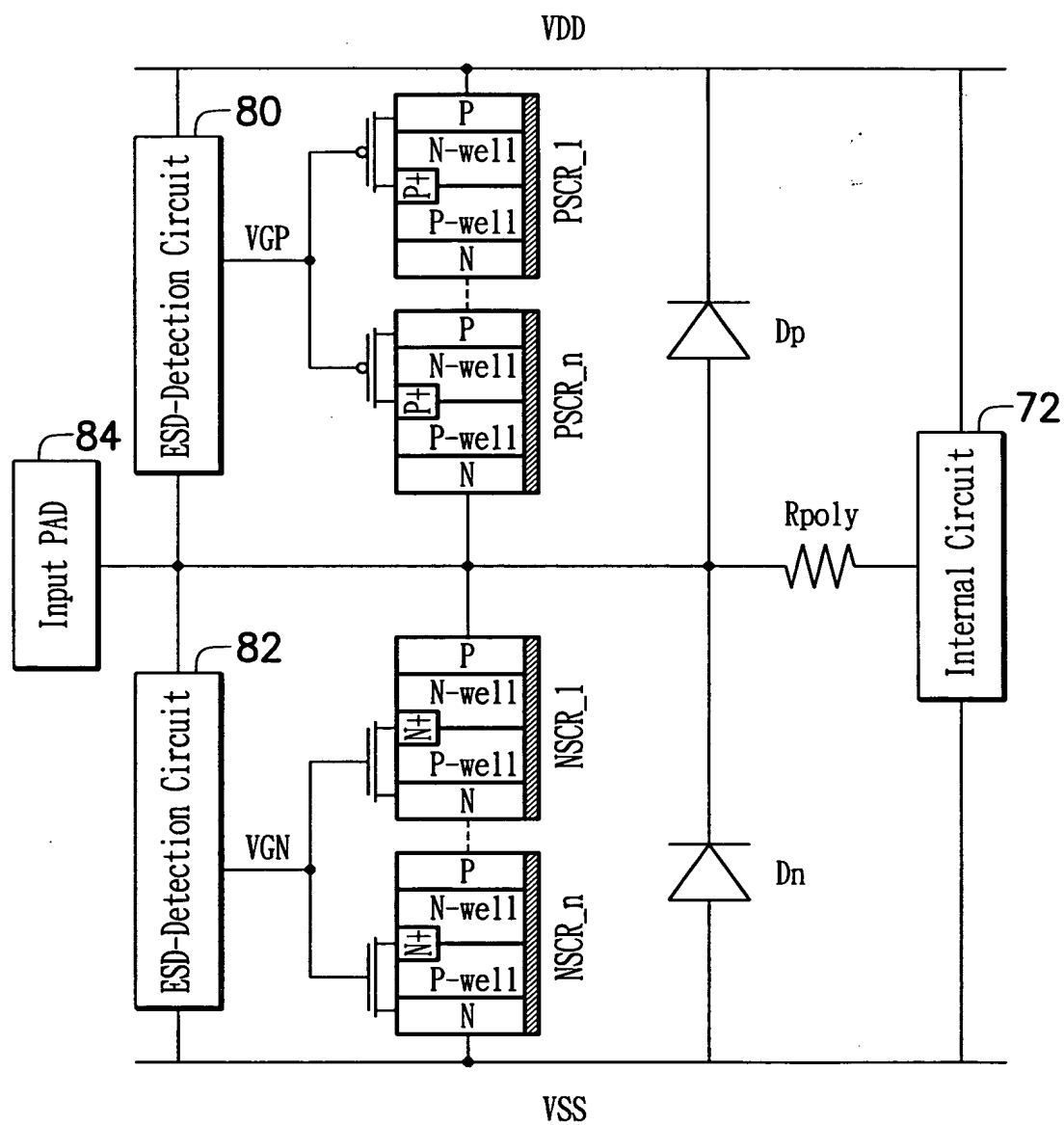


FIG. 16

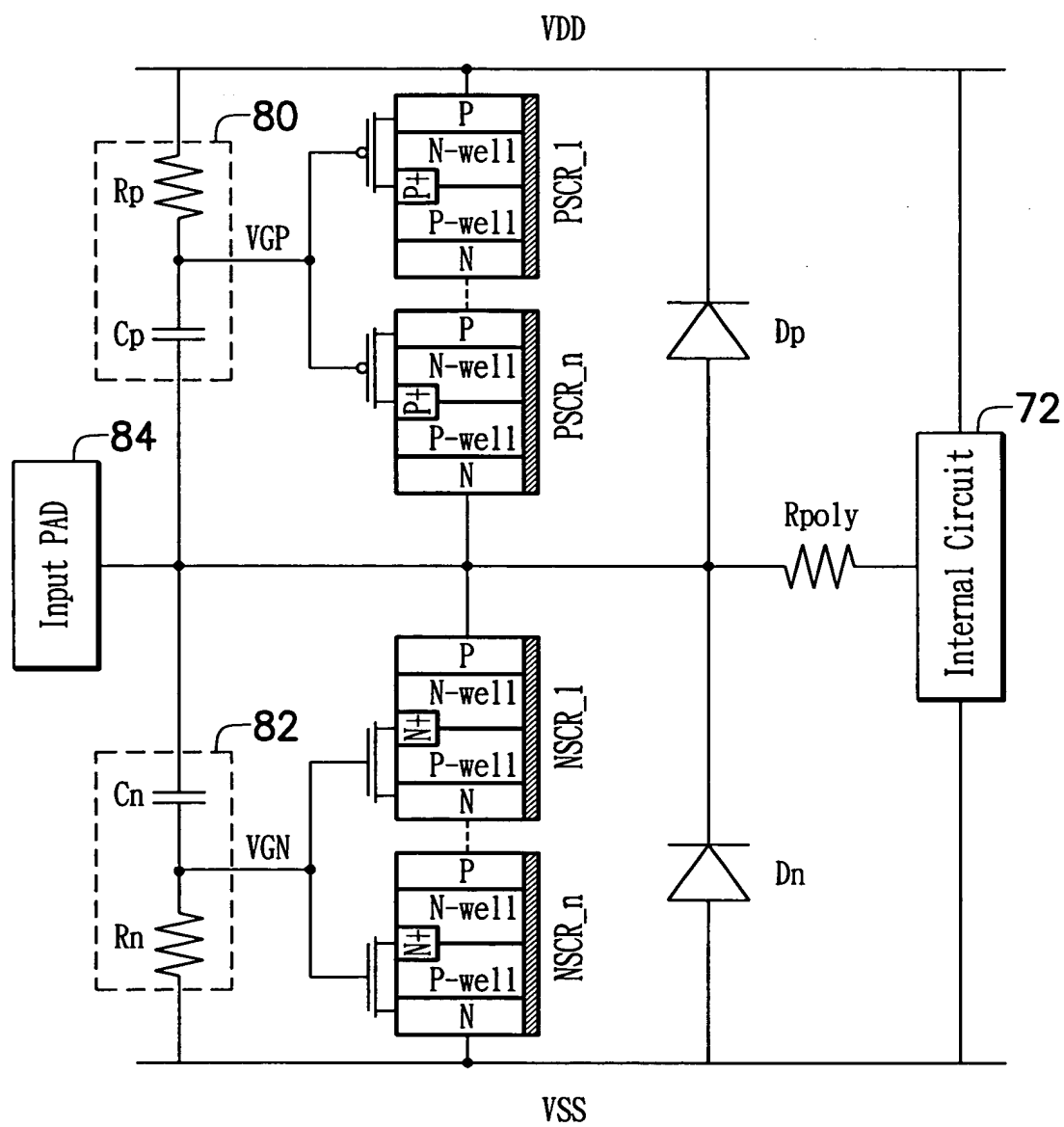


FIG. 17

FIG. 18

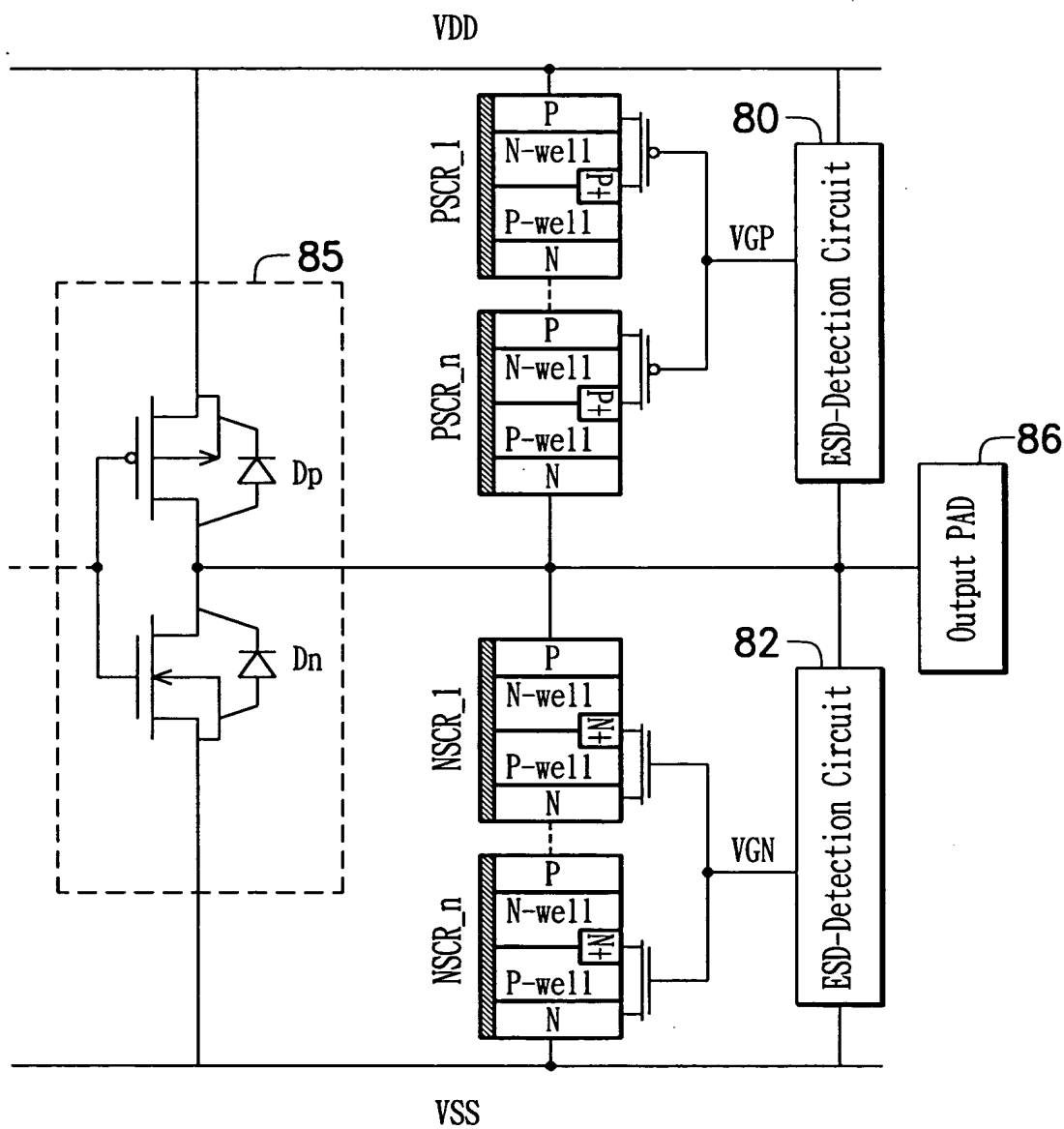


FIG. 18

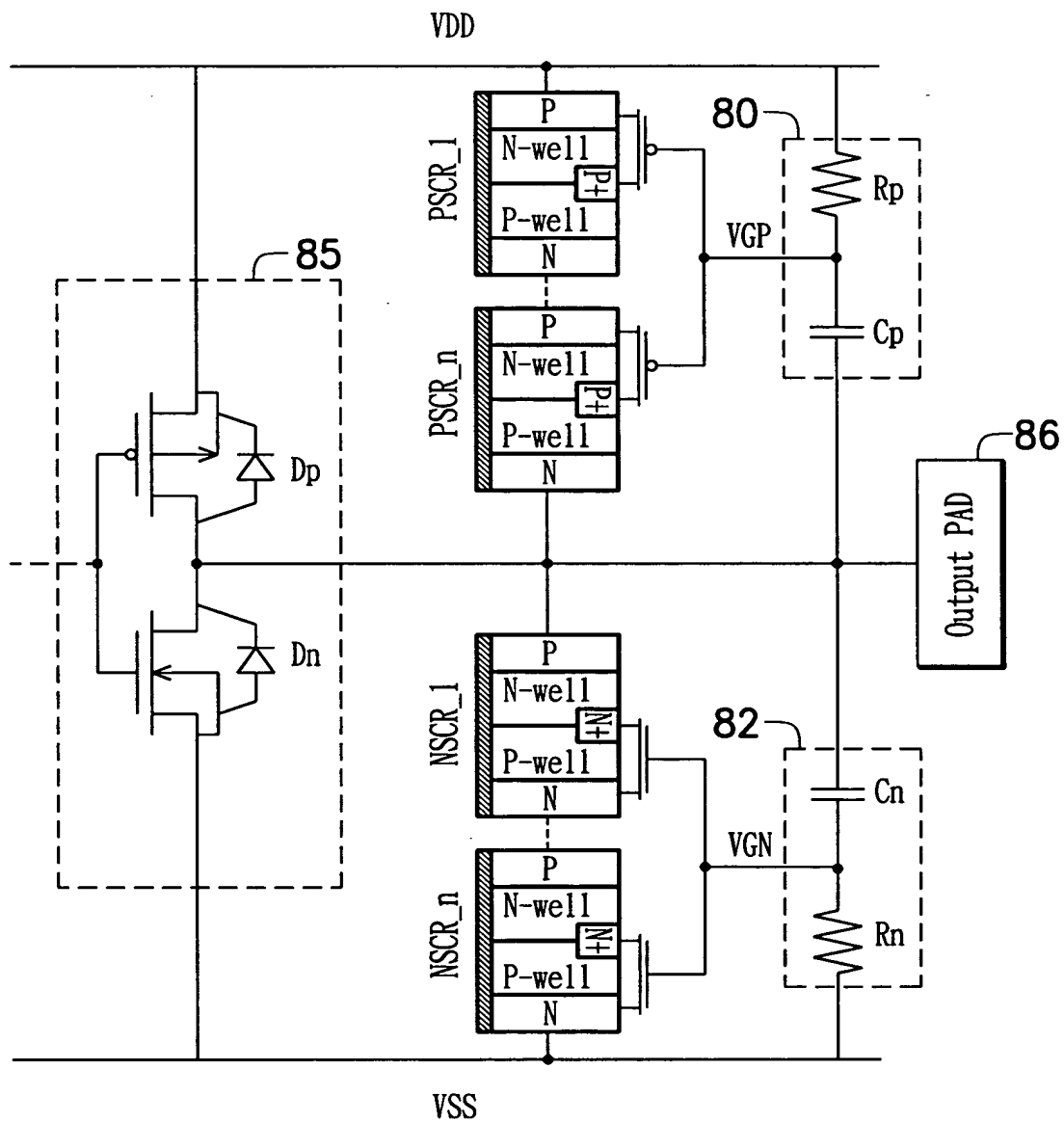


FIG. 19

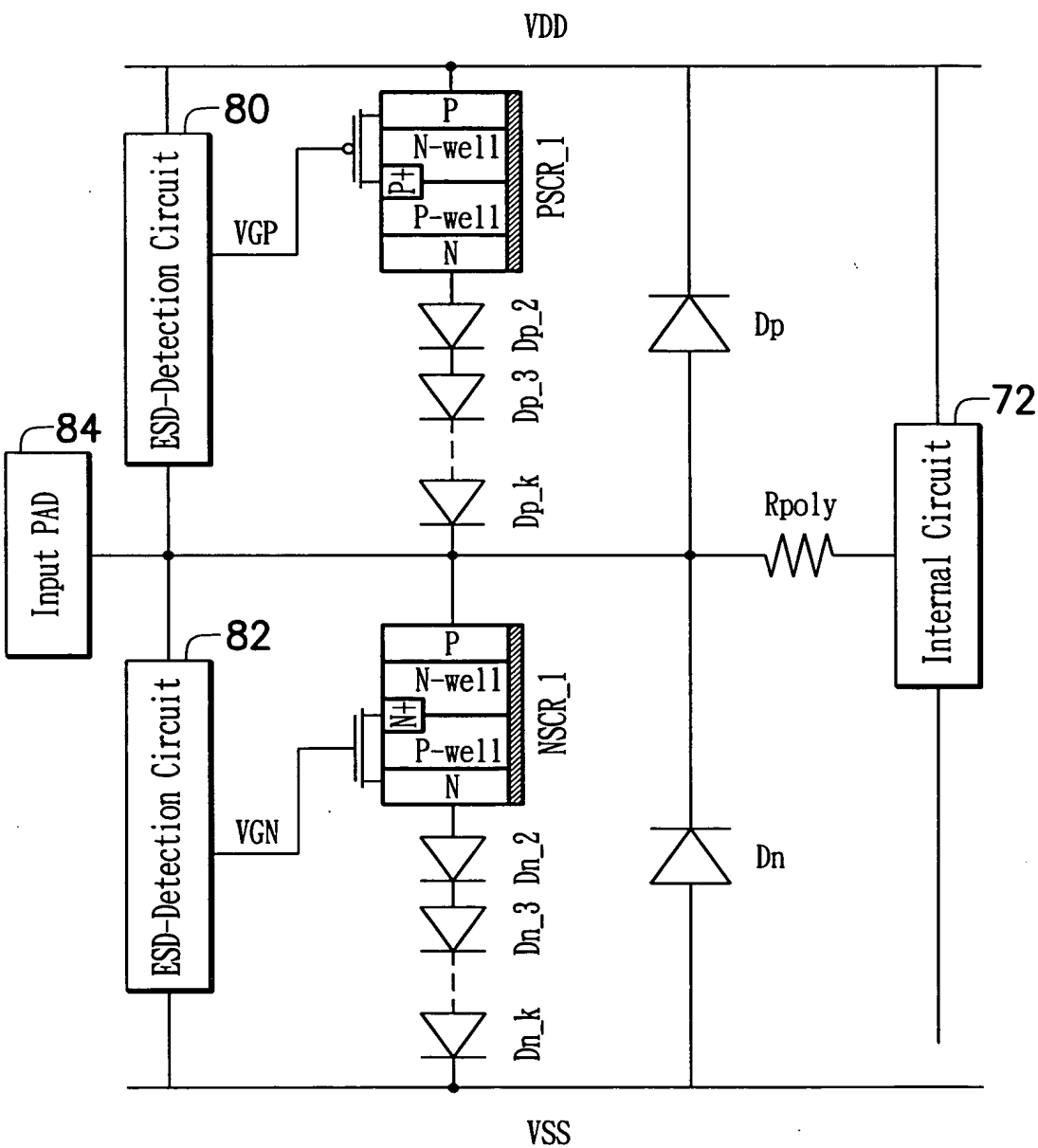
[illegible]

FIG. 20

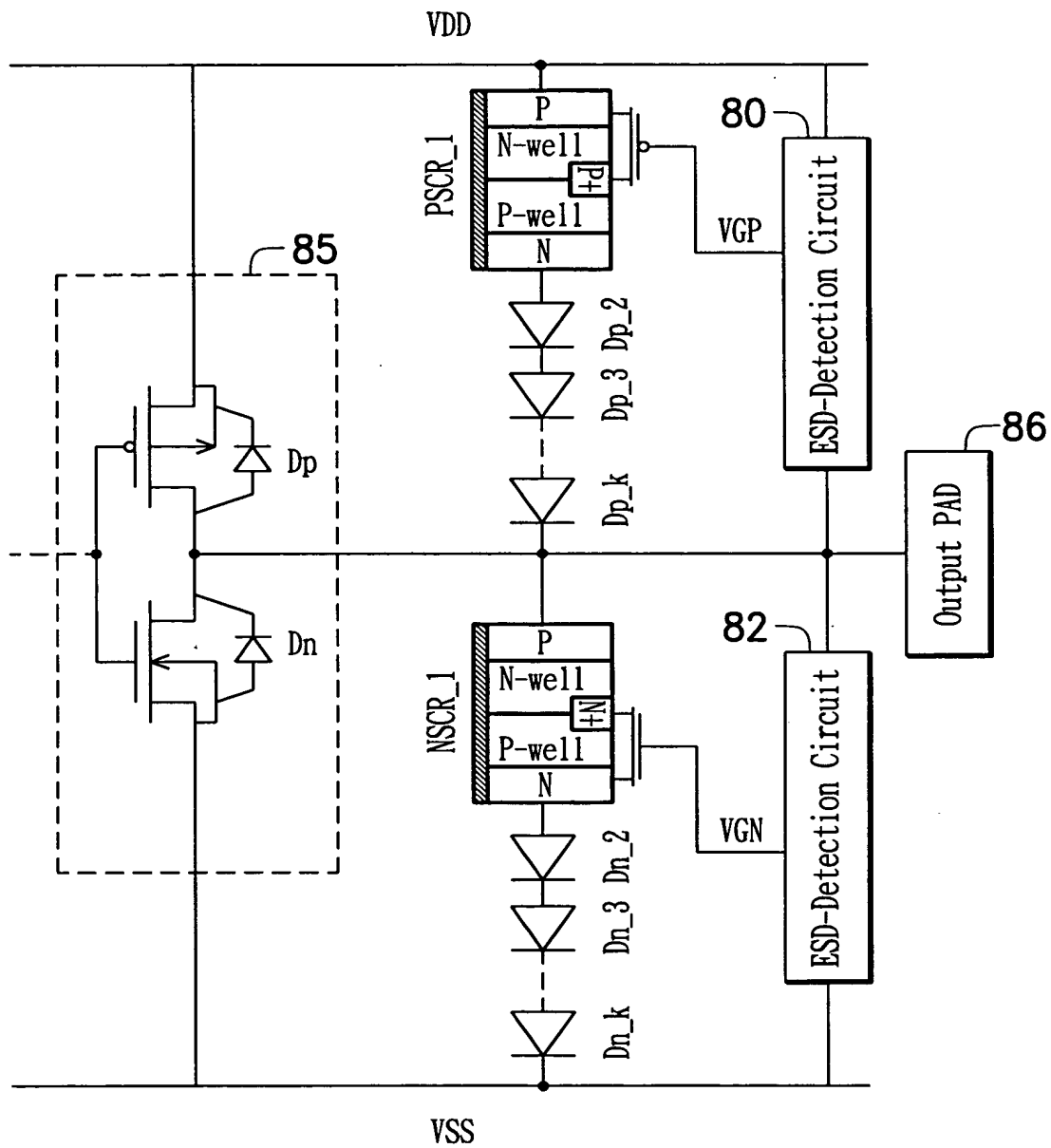


FIG. 21

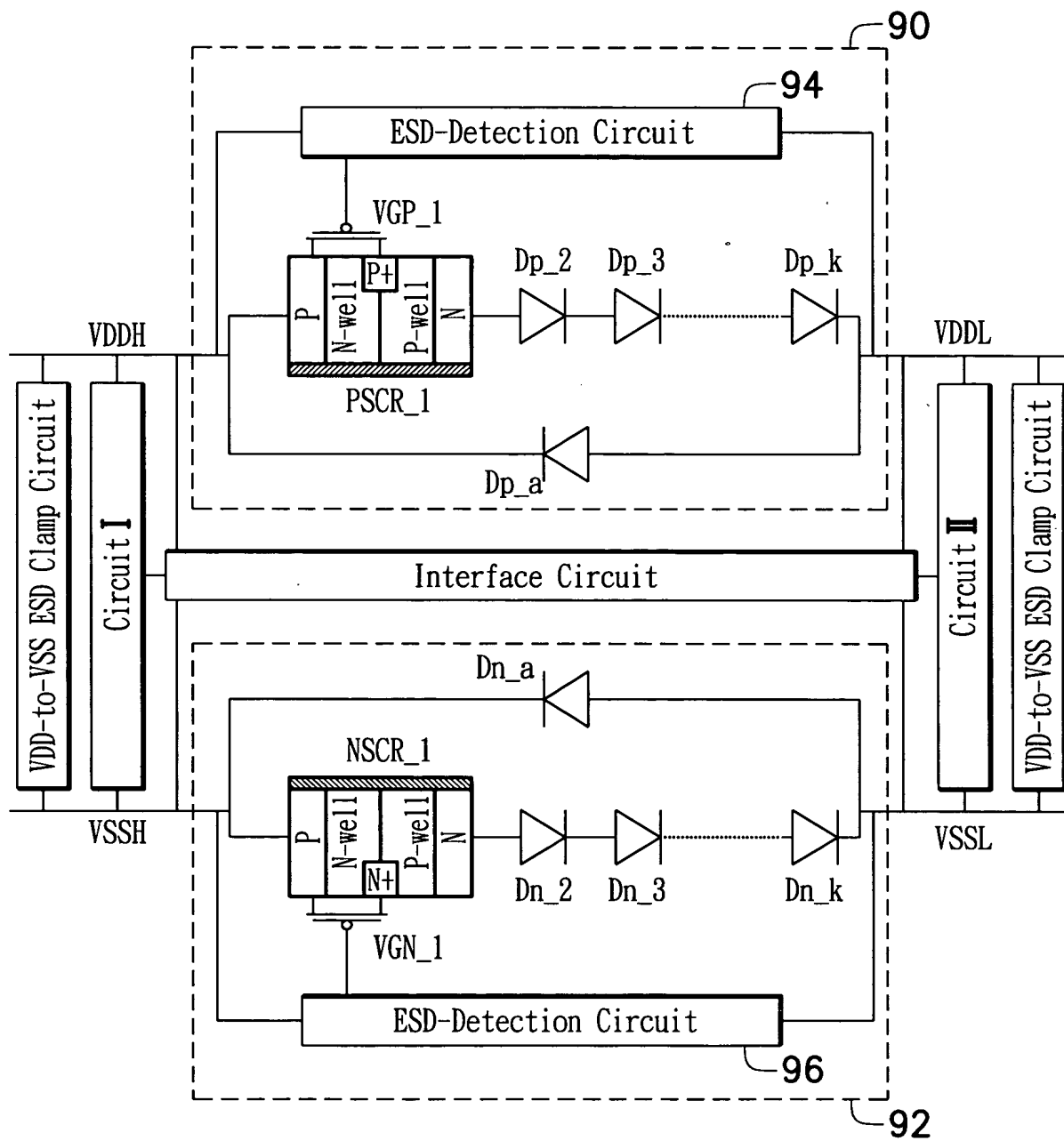


FIG. 22

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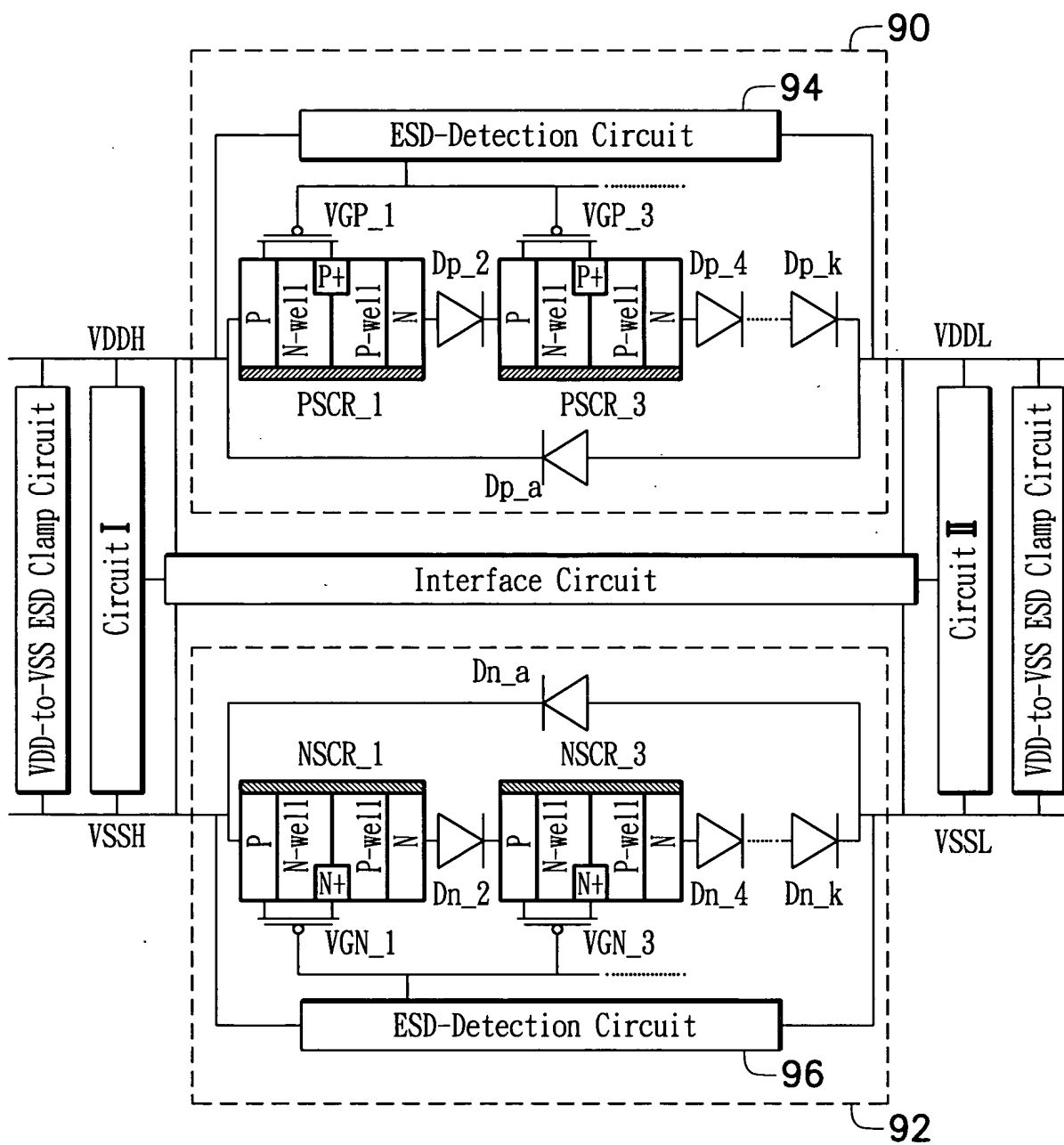


FIG. 23